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CLOCK DISTRIBUTION METHOD

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### Claim

For a method for distributing the clock of a first and a second clock supply source to a speech path device of a digital exchange device, a clock distribution method characterized in that a master clock and a clock switching circuit are arranged in the path from each clock supply source to the speech path device within the digital exchange device; the first clock supply source is connected to the first input unit of a first and a second clock switching circuit via a first master clock circuit; the second clock supply source is connected to the second input unit of the first and the second clock switching circuit via a second master clock circuit; the output units of the first and second clock switching circuits are connected respectively to first and second input units of selection circuits in the speech path device; one of the clocks supplied from the first and second clock supply sources is supplied to the first and second input units of the aforementioned selection circuit by classifying the input information by means of the switching information unit of the aforementioned clock switching circuits; and one of the clocks supplied to the first and second units of the selection circuit is selected and output from the output unit of said selection circuit.

### Detailed explanation of the invention

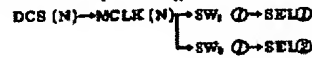
The present invention pertains to a method for distributing the clock to a speech path device in a digital exchange device for which the clock distribution method is facilitated.

A conventional clock distribution method is structured as shown in Figure 1. In Figure 1, DCS(N) is a first clock supply source, DCS(E) is a second clock supply source, TDX is a digital exchange device, MCLK(N) is a first master clock circuit, MCLK(E) is a second master clock circuit, SPE<sub>1</sub> and SPE<sub>n</sub> are speech path devices, SEL is a selection circuit, and ① and ② are first and second input units. With this method, clock supply source DCS(N) is usually used, and when it is not functioning, a clock is supplied from clock supply source DCS(E). When the clock supply source DCS(N) fault is eliminated, clock supply source DCS(N) again supplies the clock. In addition, the two clocks supplied by the digital exchange device TDX are received by master clocks MCLK(N) and MCLK(E) and the clocks are distributed without change to speech path devices SPE<sub>1</sub>-SPE<sub>n</sub> as two lines and one of the two clocks is selected at the selection circuit SEL and is used by each speech path device. In addition, a clock interruption detection circuit is located in front of selection circuit SEL (it is not shown in the figure, but its location corresponds to the first input unit ① and second input unit ② of selection circuit SEL in Figure 1) and it constantly monitors the input clock. Accordingly, for example when the clock supply line DCS(N) → MCLK(N) → SEL ① is used and when a clock interruption is detected by either of the clock interruption detection circuits of this clock supply line, the clock supply line is inverted and the clock is supplied by the clock supply line DCS(E) → MCLK(E) → SEL ②. Here, because the phases of the clock from clock supply source DCS(N) and the clock from clock supply source DCS(E) differ, a loss in synchronization occurs for short periods of time in the digital exchange device TDX. Thus with the conventional method, whenever a fault occurs in a portion of the clock supply lines, the clock supply lines must be inverted, which makes maintenance more difficult. Moreover, the loss in synchronization in the digital exchange device for short periods of time during inversion is unsuitable, and the reliability of this clock supply system is unsuitable when it is implemented on a large scale. Furthermore, the management demarcation and the maintenance demarcation are different for the digital exchange device and clock supply sources DCS(N), DCS(E), so they must be clearly classified with respect to an interface. But as above, because the clock supply line must also be switched when a fault occurs with speech path devices SPE<sub>1</sub>-SPE<sub>n</sub>, this objective cannot be achieved.

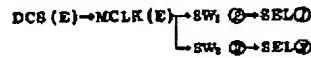
The present invention is characterized in that classification of the interface is clarified using the clock switching circuit, thus rationalizing management of the clock distribution system to provide a clock distribution method that eliminates the aforementioned problem.

Figure 2 is one application example of the present invention; it differs from the conventional method shown in Figure 1 in that clock switching circuits SW<sub>1</sub>, SW<sub>2</sub> have been

added. By means of this construction, during normal operation, first clock supply source DCS(N) and first master clock circuit MCLK(N) operate, and when first clock switching circuit SW<sub>1</sub> and second clock switching circuit SW<sub>2</sub> receive, via a terminal RT, a specific input information classification (for example, a '1' clock) that is generated by an input information classification creation circuit (not shown in the figure), a clock is supplied to the input units ①, ② of selection circuit SEL of each speech path device SPE<sub>1</sub>-SPE<sub>n</sub> as shown below:



In addition, when a fault occurs with either the first clock supply source DCS(N) or the first master clock circuit MCLK(N), it is detected by a fault detection circuit (not shown in the figure), on the basis of which first and second clock switching circuits SW<sub>1</sub> and SW<sub>2</sub> receive, via terminal RT, a specific input information classification (for example, a '2' clock), so a clock is supplied to the input units ①, ② of selection circuit SEL of each speech path device SPE<sub>1</sub>-SPE<sub>n</sub> as shown below:



Furthermore, when a fault occurs for example with the first input unit ① of switching circuit SEL of SPE<sub>1</sub> of speech path devices SPE<sub>1</sub>-SPE<sub>n</sub> and this fault is detected by the clock interruption detection circuit (not shown in the figure) that is located in front of this selection circuit SEL, the selection circuit SEL of speech path device SPE<sub>1</sub> for which this fault has been detected is operated and speech path device SPE<sub>1</sub> uses the clock received by the second input unit ②, so no adverse effect due to a phase difference occurs, as it does with the conventional method. Furthermore, as explained above, a clock from a single supply source, DCS(N) or DCS(E), is supplied constantly to input units ①, ② of switching circuit SEL of speech path devices SPE<sub>1</sub>-SPE<sub>n</sub>; therefore, when no fault occurs with input units ①, ② of the individual speech path devices, the clock can be selected and used freely by input unit ① or ②.

Furthermore, said speech path devices can operate only their own selection circuit SEL, so an advantage is achieved in that no impact is received from the other. In addition, faults other than those with switching circuits SW<sub>1</sub>, SW<sub>2</sub> are handled by the digital exchange device TDX.

As explained above, by means of the present invention by providing clock switching circuits SW<sub>1</sub>, SW<sub>2</sub> after master clock circuits MCLK(N), MCLK(E), management of the clock distribution system of clock supply sources DCS(N), DCS(E) and management of the clock distribution system within digital exchange device TDX can be separated, thus clarifying the interface. Furthermore, the clock is distributed to speech path devices SPE<sub>1</sub>-SPE<sub>n</sub> continually with two lines from a single clock supply source, so the clock distribution system can be managed independently for speech path devices SPE<sub>1</sub>-SPE<sub>n</sub>; accordingly, management of the clock distribution system is facilitated. Furthermore, a clock that is operating normally can be

freely selected by means of the selection circuit SEL, independently for speech path devices  $SPE_1$ - $SPE_n$ ; thus an excellent effect with respect to reliability can be obtained as well.

#### Brief description of the figures

Figure 1 is a block diagram for the purpose of explaining a conventional clock distribution method. Figure 2 is a block diagram of one application example of the present invention.

#### Explanation of symbols

DCS(N), DCS(E)	Clock supply source
MCLK(N), MCLK(E)	Master clock circuit
$SW_1$ , $SW_2$	Clock switching circuit
$SPE_1$ , $SPE_n$	Speech path device

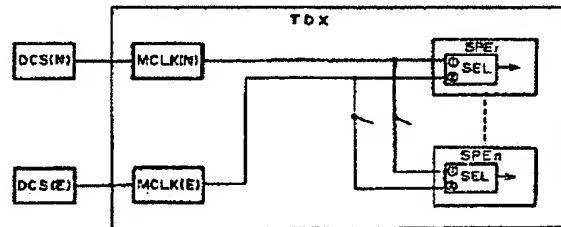


Figure 1

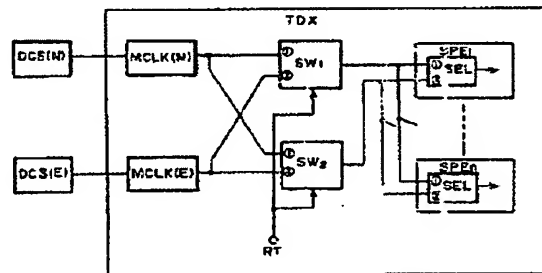


Figure 2

⑬ 日本国特許庁 (JP)

⑭ 特許出願公開

## ⑬ 公開特許公報 (A)

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(全 3 頁)

## ⑰ クロック分配方式

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⑰ 出 願 昭53(1978)10月18日  
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## 明 細 書

## 1. 発明の名称

クロック分配方式

## 2. 特許請求の範囲

第1および第2のクロック供給源のクロックをデジタル交換機の通話路系装置へ分配する方式において、各クロック供給源から通話路系装置に至るデジタル交換機内の経路にマスタクロック回路およびクロック系切替回路を配置し、第1のクロック供給源は第1のマスタクロック回路を介して第1および第2のクロック系切替回路の第1の入力部に接続し、第2のクロック供給源は第2のマスタクロック回路を介して第1および第2のクロック系切替回路の第2の入力部に接続し、第1および第2のクロック系切替回路の出力部は通話路系装置内の選択回路の第1および第2の入力部にそれぞれ接続し、前記クロック系切替回路の切替情報入力部の入力情報種別により第1および第2のクロック供給源から供給されるクロックの1方を前記選択回路の第1および第2の入力部に

(1)

与え、該選択回路の出力部から選択回路の第1および第2の入力部に与えられたクロックの1方を選択して出力することを特徴とするクロック分配方式。

## 3. 発明の詳細な説明

本発明はクロック分配系の管理を容易にしたデジタル交換機における通話路系装置に対するクロック分配方式に関するものである。

従来のクロック分配方式は第1図で示すように構成されている。即ち、第1図において、DCS(N)は第1のクロック供給源、DCS(E)は第2のクロック供給源、TDXはデジタル交換機、MCLK(N)は第1のマスタクロック回路、MCLK(E)は第2のマスタクロック回路、SPE<sub>1</sub>およびSPE<sub>2</sub>は通話路系装置、SELは選択回路でその①、②は第1および第2の入力部である。この方式では、通常はクロック供給源DCS(N)が使用され、その機能が停止するとクロック供給源DCS(E)からクロックが供給される。クロック供給源DCS(N)の障害が回復すると再びクロック供給源DCS(N)がクロックの供給を行なつて

(2)

( 3 )

DCS (N) → MCLK (N) → SW<sub>1</sub> ① → SEL①

として、第1のクロック供給源 DCS(N)と第1のマスタクロック回路 MCLK(N)のいずれか一方で障害が発生すると障害検出回路(図示省略)で検知し、これに基づく特定の入力情報種別(例えば“2”のクロック)を端子RTを經由して第1および第2のクロック系切替回路 SW<sub>1</sub>、SW<sub>2</sub>が受けることによつて、通話路系装置 SPE<sub>1</sub> ~ SPE<sub>n</sub>は各々の選択回路 SELの入力部①、②に以下のようにしてクロックが供給される。

$$\begin{array}{l}
 \text{DCS(E)} \rightarrow \text{MCLK(E)} \rightarrow \text{SW}_1, \text{②} \rightarrow \text{SEL①} \\
 \hspace{15em} \downarrow \\
 \hspace{15em} \text{SW}_2, \text{②} \rightarrow \text{SEL②}
 \end{array}$$

( 5 )

第2図は本発明の1実施例であつて、第1図で示した従来方式とはクロック系切替回路 $SW_1$ 、 $SW_2$ を付加した点が異なる。この構成により、正常時は、第1のクロック供給源 $DCS(N)$ と第1のマス

( 4 )

以上説明したように、本発明によればマスクク

( 6 )



特開 昭55-53956 (3)

ロック回路 MCLK(N)、MCLK(E) の後位にクロック系切替回路 SW<sub>1</sub>、SW<sub>2</sub> を配置したことによつて、クロック供給源 DCS(N)、DCS(E) のクロック分配系管理とデジタル交換機 TDX 内のクロック分配系管理が分離し、インタフェースが明確になつた。また、通話路系装置 SPE<sub>1</sub> ~ SPE<sub>n</sub> へのクロック分配を単一のクロック供給源から常時 2 系統で行なうのでクロック分配系の管理を通話路系装置 SPE<sub>1</sub> ~ SPE<sub>n</sub> 中の個々独立に行なうことができ、従つてクロック分配の系管理が容易となり、さらに、通話路系装置 SPE<sub>1</sub> ~ SPE<sub>n</sub> 中の個々独立にその選択回路 SEL によつて自由に都合のよい方のクロックを選択できるので信頼性上も好ましい結果が得られる。

#### 4. 図面の簡単な説明

第 1 図は従来のクロック分配方式を説明するためのブロック図、第 2 図は本発明の 1 実施例に係るブロック図である。

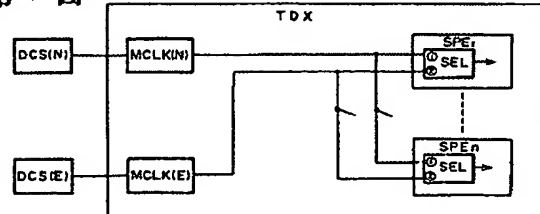
DCS(N)、DCS(E) ……クロック供給源、MCLK(N)、MCLK(E) ……マスタクロック回路、SW<sub>1</sub>、SW<sub>2</sub> ……クロック系切替回路、SPE<sub>1</sub>、SPE<sub>n</sub> ……通話路系装置。

(7)

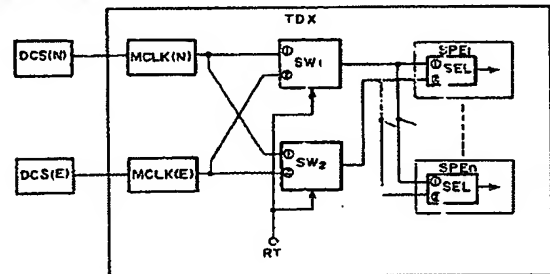
#### 第 1 頁の続き

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第 1 図



第 2 図



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## (54) CLOCK DISTRIBUTION SYSTEM

## (57)Abstract:

PURPOSE: To ensure the rational control for the clock distribution system by providing the clock system switching circuit after the master clock circuit.

CONSTITUTION: Clock system switching circuits SW1 and SW2 are provided after master clock circuits MCLK(N) and MCLK(E). As a result, an isolation is secured between the clock distribution system control of clock supply sources DCS(N) and DCS(E) and the clock distribution system control within digital exchange TDX. Thus the interface is made clear. Furthermore, the clock distribution to channel system devices SPE1 ~ SPEn is carried out from the single clock supply source and in two systems at all times, and as a result the control of the clock distribution system can be performed independently among devices SPE1 ~ SPEn. Accordingly, the system control can be facilitated for the clock distribution.

